Employment of Microwave Absorbers for EMI/RFI mitigations from High Speed Digital Buses with Signal Integrity Considerations

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***Abstract*—An analysis of electromagnetic radiation reduction achieved by placement of microwave absorbers over a serial high speed digital channel is performed. The study is performed on a second generation peripheral component interconnect express (PCIe Gen II) interface with 5.0 Gbps transfer rate. A set of full wave simulations are performed on a printed circuit board with the PCIe interface implemented in an embedded micro-strip line structure. Lossy material patches are applied onto the channel to reduce the electromagnetic radiations from differential pairs. This reduction might be required especially in compact mixed signal systems as noisy digital circuits are located close to radio-frequency receivers with stringent sensitivity limits. Using the numerical solver, it has been shown that the application of the absorber can reduce the magnitude of the received electromagnetic fields at the desired locations while unfortunately affecting the signal integrity performance of the bus. In order to reduce the unintentional discontinuity introduced along the differential pairs as applying the material on the PCB, the insertion of a dielectric spacer sheet between the absorber and the solder mask is investigated. It has been shown that the presence of a thin layer of the spacer (less than 0.2mm) can significantly decrease the introduced mismatch while still keeping the benefit of the EM reduction. Full wave simulation results are being confirmed by near field probing set-up and a PCIe compliance test board.**

Keywords—absorbers; electromagnetic compatibility; radio frequency interference; signal integrity.

I. INTRODUCTION

Recently, intra-system electromagnetic interference and its related problems are becoming more critical as many mixed signal systems with digital integrated circuits (ICs) and their peripherals are placed in the vicinity of radio frequency analog receivers (such as Bluetooth, Wi-Fi, GPS etc.) in small form factors [1]-[9]. The radio frequency (RF) front-end circuits of analog receivers, usually consisted of a low noise amplifier, are very sensitive to the input noise at their designed bandwidth. In a highly integrated system such as handsets, this noise mostly originates from adjacent switching drivers and clocks. The undesired interference can manifest through the radiated emissions of heat sinks, bus or high speed clock traces (routed on the outer layers of the PCB) or noisy integrated ICs coupled to a receiving antenna [4]. The receiver desensitization can also occur due to the electromagnetic (EM) wave propagation generated by the switching microprocessors through parallel power planes [7].

This intra-system electromagnetic coupling also called radio frequency interference (RFI) is mostly characterized through the receiver power measurement by the receiver under test antenna as it is separated from the device input. The desired sensitivity levels of several embedded wireless standards (that can be measured by a spectrum analyzer) are detailed in Table I with specified resolution bandwidths [7]. As can be seen in Table I, there are desired noise levels as low as -115 dBm.

To understand the importance and need of radio receiver placement and digital noise mitigation for minimizing related RFI issues, a simple but intuitive experiment is designed. A 50 Ω micro-strip line (50mm length) is fabricated on a 1.5mm thick RT-5880 substrate (see Fig. 1). The micro-strip line is terminated with a matched coaxial load in one end and excited through a sinusoidal and continuous source set to 2.45 GHz (near to the WLAN band center 2412-2482 MHz) at -40 dBm power. The radiated electromagnetic power from the 50 Ω terminated trace is captured by an antenna (designed and tested for the WLAN band), and measured using a preamplifier and a spectrum analyzer. In addition, the distance between the antenna and the micro-strip line is being changed to find the minimum required spacing to detect maximum acceptable noise level in WLAN specification defined at -115 dBm. It is expected that the matched single ended transmission line with a perfect ground plane underneath would not pose any electromagnetic compatibility threat in the far field region around 2.4 GHz WLAN band. However, the measured received power at 2.4 GHz can reach up to the WLAN RFI noise limit within distances up to 270 mm from the radiator. This simple experiment highlights the challenges that RFI engineers face while designing a compact mixed signal system. To further explore this simple example, the top surface of the micro-strip line was completely covered with a microwave

absorber (BSR20 [11]). It was determined the clearance criteria reduces to 220 mm due the presence of the lossy material.

Table I: Common RFI specifications of popular wireless communication standards.

BANDS (MHz)	Radio Standard	Measure RBW	Freq Range Start	Freq Range Stop	Specification
LTE Band 13	LTE	10 MHz	746 MHz	756 MHz	-95 dBm
850	GSM, CDMA, EV-DO, WCDMA	200 kHz	869 MHz	894 MHz	-108 dBm
900	GSM	200 kHz	925 MHz	960 MHz	-108 dBm
1.575 GHz	GPS / GLONASS	100 kHz	1540 MHz	1620 MHz	-114 dBm
1800	GSM	200 kHz	1805 MHz	1880 MHz	-108 dBm
1900	GSM, CDMA, EV-DO, WCDMA	200 kHz	1930 MHz	1990 MHz	-108 dBm
2100	WCDMA	5 MHz	2110 MHz	2170 MHz	-97 dBm
2400	WLAN 2.4G	100 kHz	2400 MHz	2480 MHz	-115 dBm
LTE High Band	LTE	10 MHz	2300 MHz	2650 MHz	-95 dBm
5100	WLAN 5G	100 kHz	5100 MHz	5800 MHz	-115 dBm

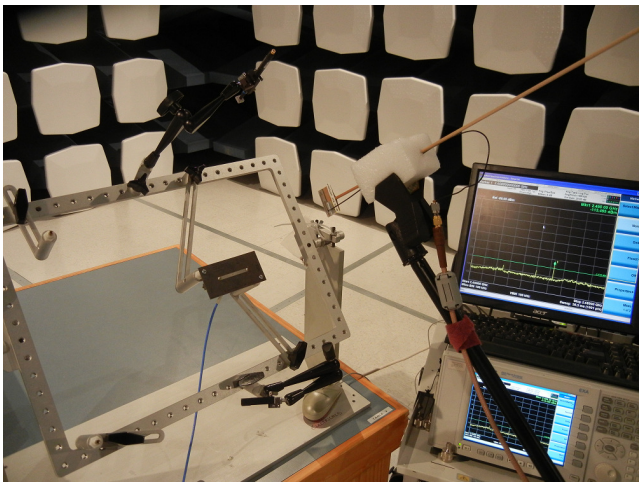


Fig. 1: A simple test designed to examine RFI limits for WLAN band. The radiated EM waves from a terminated micro-strip line are detected using WLAN band antenna.

In this paper, EM radiation and signal integrity performance of a reference platform provided by [11] with an active second generation peripheral component interconnect express (PCIe Gen II), mostly implemented on the top layer of the PCB as micro-strip line structure, is considered. To this end, different measurements and simulations are performed after applying various types and thicknesses of absorber sheets onto the PCIe micro-strip traces that are running on the top layer of the PCB. For the simulation, a full wave simulation tool [12] is employed to characterize the transmitting pairs of the PCIe channel running from an accelerated processing unit (APU) to a receiver IC on a graphics processing unit (GPU) card. Near field probe measurements are performed before and after the absorber application while using a preamplifier to clearly detect the radiated field changes above the PCIe bus. Additionally, a PCIe compliance load board and a real time oscilloscope is used to measure the eye diagram variations as different absorbing materials are applied. These tests are repeated after inserting a dielectric spacer between the lossy material and the PCB. It is shown that a specific absorber type can effectively reduce the radiated fields over a wide frequency range and minimally affect the measured eye diagram when a dielectric spacer is employed.

II. Measurement and Simulation Set-up

A. *Measurement set-up*

The platform under test is chosen for this research since it provides several latest I/O interfaces including USB 3.0, PCIe Gen III, and SATA III in addition to sensitive analog receivers such as GPS, WLAN and WWAN. We have chosen PCIe bus since its wide-band generated noise coincides with most commonly used radio receiver spectrum. Additionally, it is easily accessible for near field probing and the application of RFI mitigation solutions is also easier on it since it is implemented on the outer layers of the PCB. To maximize the emissions from the differential traces of the PCIe bus, spread spectrum is disabled while a benchmarking software (Unigine Heaven with 1920 × 1200 resolution and 60 Hz refresh rate) is used to exercise the graphics card mounted on the PCIe slot of the motherboard

Specific electric and magnetic probes that allow measurements in the frequency range of 30 MHz to 6 GHz are chosen such that they have a spatial resolution of 2mm (H-field) and 10mm (E-field) [13]. Near field probe measurements are conducted inside a 10m EMI anechoic chamber to eliminate ambient noise. Detected radiated fields are further amplified with a pre-amplifier with 44 dB gain and are measured using a FFT spectrum analyzer (N9010A) in Max-hold mode with frequency span of 20 MHz and resolution bandwidth of 1 MHz.

To examine the placement of the absorber over the PCIe channel two absorbers composed of magnetically loaded elastomers with: (a) spherical shaped (BSR 20), and (b) platelets (NS1040) ferrite inclusions, with respective thicknesses of 0.63mm and 0.47 mm are employed [10]. In order to determine the effects of the addition of a spacer between the absorber and the PCB on its EMI reduction functionality and SI degradation, a 0.13 mm thick paper-based dielectric is employed. Fig. 2 depicts a view of the tested platform with NS1040 absorber placed over the PCIe transmit lanes with an E-field probe placed on top of the absorber during the tests.

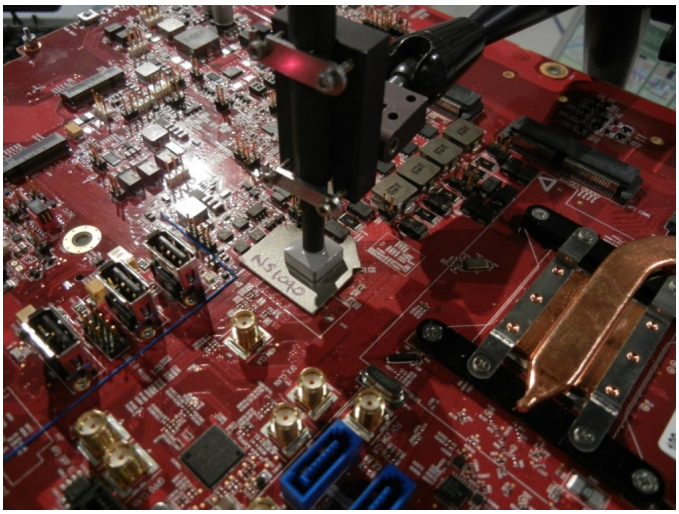


Fig. 2. A view of the platform with a sheet of a microwave absorber placed over the top-layer PCIe signal traces. An electric field probe is used to measure radiated field.

To verify link performance with and without absorber, standard signal integrity compliance tests for PCIe Gen II, as developed by PCI Special Interest Group (PCI-SIG) [15], are conducted. A compliance load board (CLB) is inserted into the PCIe connector of the motherboard. Making use of the fact that the layout for all eight transmit/receive pairs is roughly symmetrical, one set of transmit/receive pair (specifically, TX3/RX3) is selected for signal integrity check. This set is connected to a 4-channel digital oscilloscope (DSA 72004) through SMA connectors and the rest of the TX/RX pairs are terminated with 50 Ω terminations. The CLB is programmed to trigger a Gen II signal (with a data rate of 5.0 Gbps and a unit interval of 200ps) from the system, the eye diagrams are captured and post-processed using standard software [15].

B. Simulation set up

A series of full electromagnetic wave simulations are performed on the PCB of the mother board and graphic card with and without the presence of the lossy material. In order to include the properties of the microwave absorber into the model, measured frequency dependent permittivity and permeability are incorporated into the finite-element-method-based electromagnetic solver [12]. Later, the scattering-parameter-based models of the APU package, the PCIe connector and DC block capacitors provided by the vendors are incorporated into the channel simulation. A block diagram of the simulated sections is shown in Fig. 3, starting from the APU package and ending at the GPU.

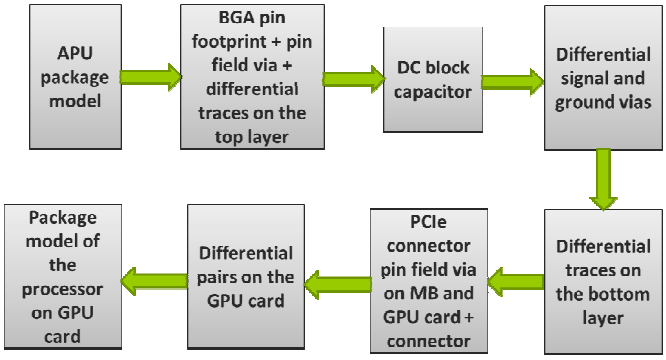


Fig. 3. A block diagram view of the simulated PCIe channel.

III. Time and Freuency Domain Simulation Results

The cascaded scattering parameters in Fig. 3 are utilized to investigate the effect of applying the microwave absorber on the PCIe bus. The results are presented in time and frequency domains in three cases: (a) without the lossy material, (b) with BSR20 placed directly on the PCIe bus, and (c) with the spacer placed between PCIe bus and BSR20.

In Fig. 4, the simulated insertion losses of three differential pairs (named GFX_TX_3, 4, 5 hereafter) for the aforementioned three cases are plotted. Additionally, the simulated power sum far-end cross-talk (PSFEXT) on a victim pair (GFX_TX_4) with adjacent aggressive pairs (GFX_TX_3 and 5) are also depicted in Fig. 4. As seen in the figure, the placement of the absorber has marginally increased the insertion loss (less than 0.4 dB) while it has reduced PSFEXT by at least 1 dB. The PSFEXT reduction happens since the EM fields have to pass through the microwave absorber instead of air above the PCB. This leads to the attenuation of the inter-pair coupling fields as they propagate through the absorber sheet.

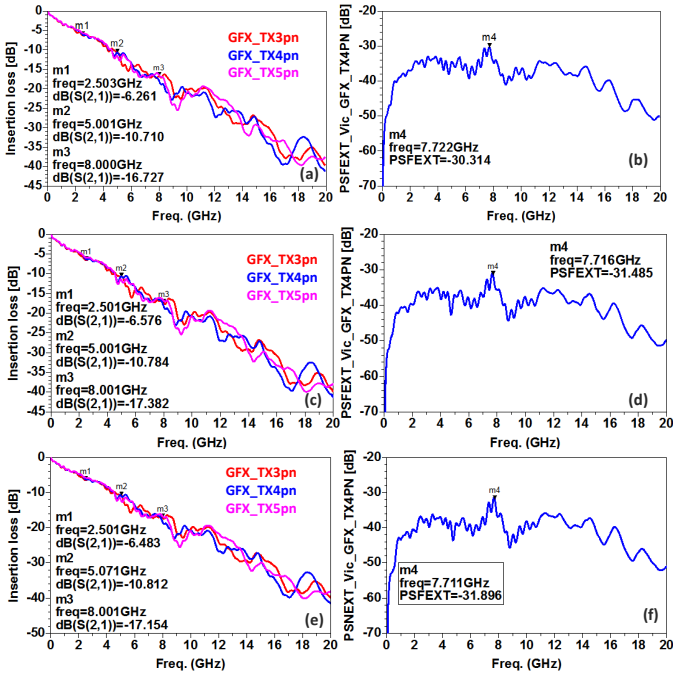
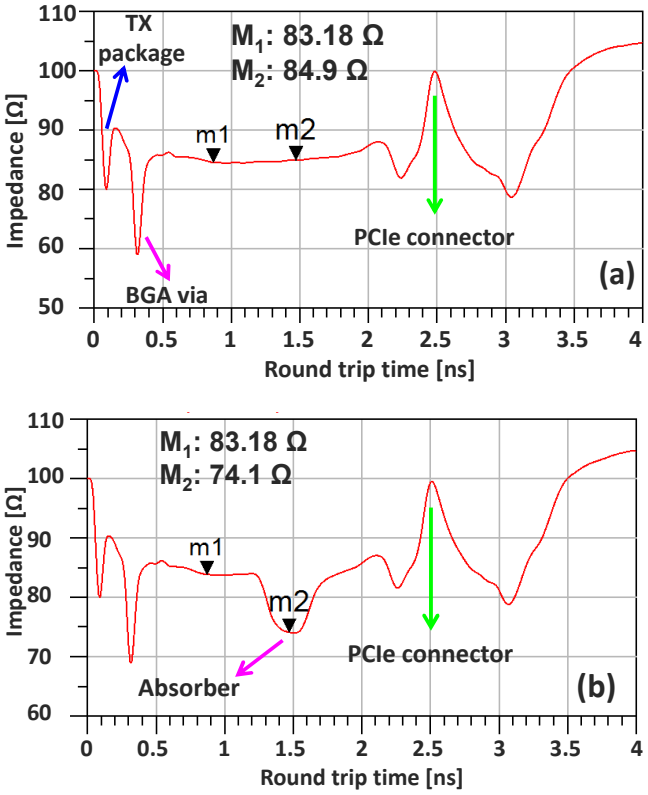


Fig. 4. The insertion losses and the power sums of the far-end cross-talks on a victim pair (a),(b) without absorber, (c),(d) and (e),(f) with BSR20 placed directly and with 0.13mm dielectric spacer over the top layer, respectively.



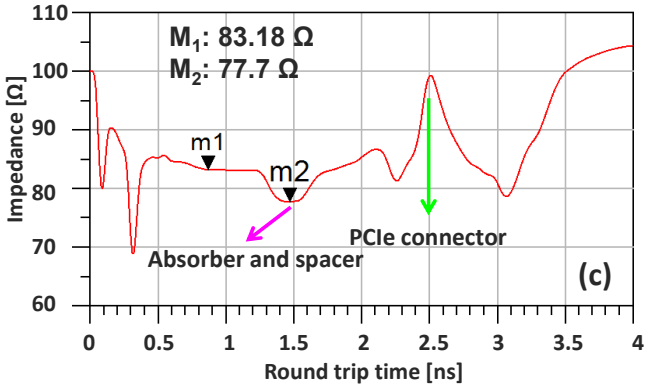


Fig. 5. Simulated input time domain reflectometry of the PCIe transmit lane from the APU side (a) without absorber, (b) and (c) with BSR20 placed directly and with 0.13mm dielectric spacer over the top layer, respectively.

To further understand the alteration of the differential signal after the placement of the microwave absorber, the input time domain reflectometry (TDR) results from the APU end are presented in Fig. 5 for the three simulated cases. TDR result in Fig. 5.(a) reveals the impedance discontinuities related to APU package model, BGA via pin field, DC block capacitor, and the PCIe connector and its footprint, as well as differential traces on the motherboard (originally designed for 85Ω) and GPU card. As seen in Fig. 5.(b), the application of the absorber directly onto the PCB has a capacitive effect on the signal which has led to a decrease of about 11Ω along the differential signal. As mentioned, a 0.13 mm thick spacer is inserted underneath the absorber in order to reduce its introduced impedance discontinuity. The performance of the spacer is illustrated in Fig. 5. (c) as the impedance change has decreased from 11Ω to 6Ω.

IV. Results of Measured Near Field Probing and Time Domain Tests

In this section, near field probing results and channel simulation results are presented. Parts of these results have been previously reported in [4]. However, they are being represented here for comparison with the simulation results. The measurements are reported into these categories: (1) baseline without any absorber, (2), (3) BSR20 with and without the paper spacer, and (4) and (5) NS1040 with and without the spacer. The reduction of the electric and magnetic fields are presented by subtracting the measured value before and after the lossy material application at the embedded clock harmonics. The measured field drops after the usage of BSR20 with and without the spacer (case 2 and 3) are depicted in Fig. 6 and 7. As can be seen, the field reduction with BSR20 is not significant particularly with the spacer. This was foreseen since this type of microwave absorber is mostly designed and utilized for cavity resonance damping applications and it is not optimized to redirect EM radiations since it does not offer very high permittivity and permeability.

In Fig. 8 and 9, radiated field reductions after placing the second absorber type (NS1040) with and without the spacer are depicted (cases 4 and 5). As seen, the absorber with very high permittivity and permeability designed for noise source

suppression can offer much better radiated field reductions both in E and H field domains up to 6 GHz.

In Table 2, the measured eye specifications and jitter values of the tested cases are presented. All measured situations have easily passed PCIe Gen II specifications. However, the reported eye opening in case 5 with NS-1040 over the PCB has been reduced up to 5ps and 0.0175V from the original case 1. However, the addition of the spacer has compensated these changes to only 1ps and 0.0022V.

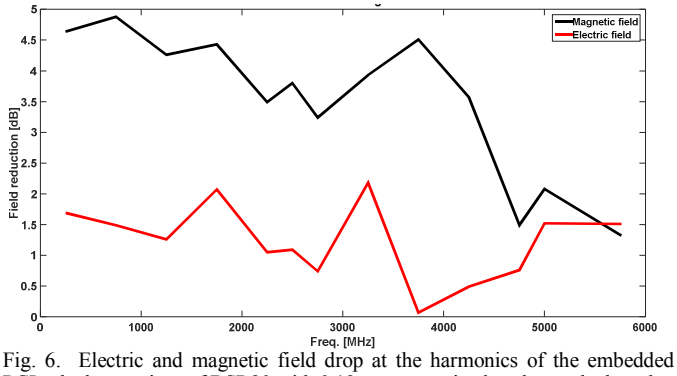


Fig. 6. Electric and magnetic field drop at the harmonics of the embedded PCIe clock as a piece of BSR20 with 0.13mm spacer is placed onto the board.

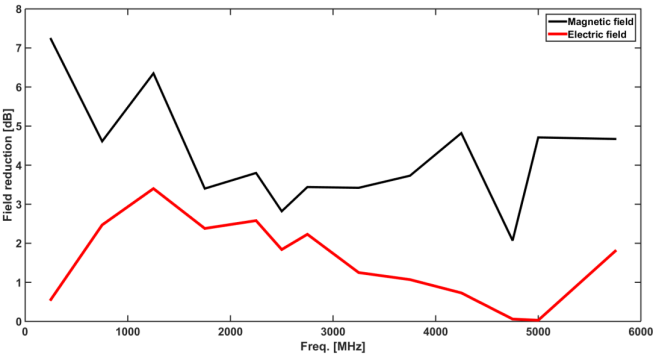


Fig. 7. Electric and magnetic field drop at the harmonics of the embedded PCIe clock as a piece of BSR20 is placed onto the board.

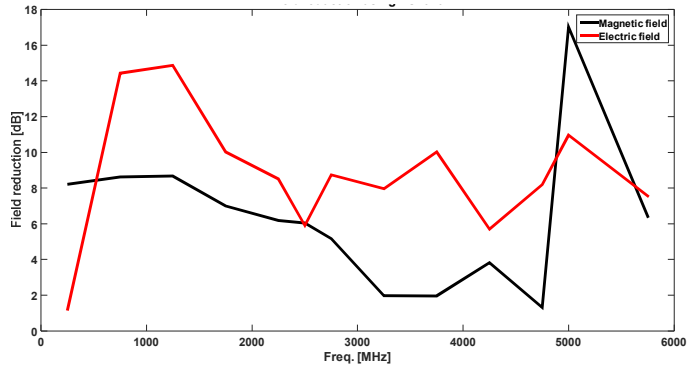


Fig. 8. Electric and magnetic field drop at the harmonics of the embedded PCIe clock as a piece of NS1040 with 0.13mm spacer is placed onto the board.

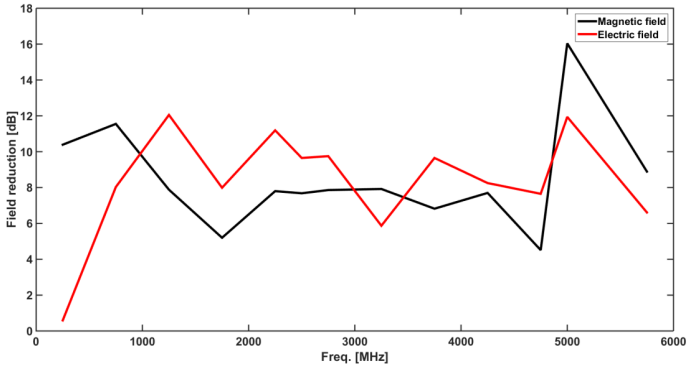
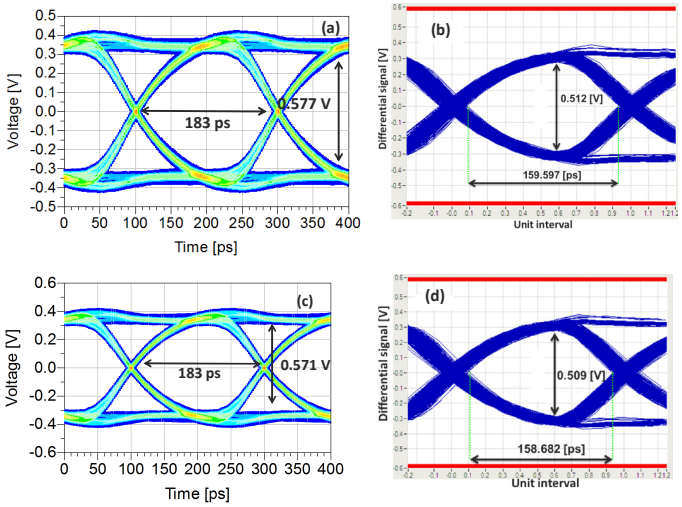


Fig. 9. Electric and magnetic field drop at the harmonics of the embedded PCIe clock as a piece of NS1040 piece is placed onto the board.

Table II: Measured eye and jitter characteristics of the PCIe channel under five different tested cases.

Cases	Max Pk-Pk Jitter (ps)	Total Jitter at BER @10E-12 (ps)	Random Jitter RMS (ps)	Deterministic Jitter Delta-Delta (ps)	Minimum Eye Width (ps)	Composite Eye Height (V)
Case 1: Baseline Measurements – Without Absorber Material	30.870	40.402	2.265	8.553	159.580	0.5125
Case 2: BSR020 with Spacer	34.121	42.527	2.433	8.316	157.473	0.512
Case 3: BSR020 without Spacer	36.570	41.318	2.224	10.042	158.682	0.509
Case 4: NS1040 with Spacer	31.270	41.331	2.330	8.580	158.670	0.5103
Case 5: NS1040 without Spacer	39.216	47.403	2.594	10.919	152.597	0.495

In Fig. 10, simulated and measured eye diagrams of the PCIe channel without and with the absorber (BSR20 placed directly and with the spacer over the board) are depicted. As seen, measured and simulated values decently compare with each other. Additionally, there are marginal reductions in the eye diagram properties, after the absorber application, which is compensated by employment of the spacer.



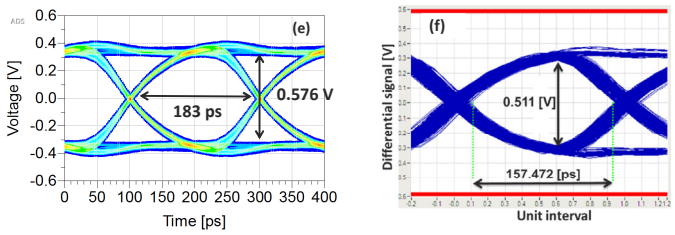


Fig. 10. A comparison between simulated and measured eye diagrams of PCIe interface (a), (b): without absorber, (c), (d) with BSR20 over the board, and (e), (f) with the spacer between the absorber and PCB.

CONSCLUSION

The usage of two types of microwave absorbers with different thicknesses placed on the top layer of a multi-layer PCB over a PCIe II differential micro-strip traces are examined in terms of timing margin variations and radiated EM field variations. It has been reported that one type of the absorbers can redirect the generated EM fields due to very high material properties. Although all measured cases have passed PCIe Gen II specifications, it has been simulated and confirmed by measurement that the insertion of a low loss dielectric can reduce the undesired discontinuities introduced by the application of the absorber. The localized use of the microwave absorber applied at sensitive areas near to analog receiver antennas can be useful as trying to pass very stringent internal RFI internal requirements in mixed signal system platforms and mobile devices.

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